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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/437,580	11/09/1999	ALEXANDER G. MACINNIS	36101/SAH/B6	8182

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EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	**PAPER NUMBER**
2674	24

DATE MAILED: 10/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/437,580	MACINNIS ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,19 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,19 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *23* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/6/2003 has been entered. An action on the RCE follows:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15, 19 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateyama "previously cited" (US 5,515,077) in view of Sokawa et al "previously cited" (US 6,353,460).

As to claim 1, Tateyama teaches the method of horizontally scrolling a display window to the left comprising the steps of

receiving a data packet (Y0 Y1 U0 V0) (figure 28) that includes a field for a blank start pixel value (Y0 U0 V0), which indicates a number of pixels to be blanked out;

blanking out one or more pixels (Y0 U0 V0) at a beginning of a portion of graphics data in accordance with the blank start pixel value;

displaying the graphics data starting at a first non-blanked out pixel in the portion of the graphics data aligned with the start address (see figure 22, column 9, lines 1-12).

Tateyama fails to teach "placing a read pointer at a location after one or more pixel, displaying the graphics data starting at the read pointer at a first non-blanked out pixel in the portion of the graphics data aligned with the start address." However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Since a pointer increments in accordance with a clock synchronized with the input image data Vs (figure 11, column 22, lines 20-22). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the read pointer taught by Sokawa et al for a read timing disclosed in the display scrolling image system of Tateyama because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 2, Tateyama teaches converting the graphics data into a common format (see column 10, line 35).

As to claims 3, 5, 6, Tateyama teaches blanking out four-bit color data (0,1,0,0) (see column 9, line 1).

As to claim 4, Tateyama teaches the common format is selected from the group of YUV and RGB formats (see figures 13 and 14, column 3, lines 60-61).

As to claim 7, Tateyama teaches the method of horizontally scrolling a display window to the right comprising the steps of

receiving a data packet (Y0 Y1 U0 V0) (figure 28) that includes a field for a blank start pixel value (Y0 U0 V0), which indicates a number of pixels to be blanked out;

blanking out one or more pixels (Y0 U0 V0) at a beginning of a portion of graphics data in accordance with the blank start pixel value;

displaying the graphics data starting at a first non-blanked out pixel in the portion of the graphics data aligned with the start address (see figure 23, column 9, lines 13-20).

Tateyama fails to teach "placing a read pointer at a location after one or more pixel, displaying the graphics data starting at the read pointer at a first non-blanked out pixel in the portion of the graphics data aligned with the start address." However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a

second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Since a writer pointer increments in accordance with a clock synchronized with the input image data Vs (figure 11, column 22, lines 20-22). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the read pointer taught by Sokawa et al for a read timing disclosed in the display scrolling image system of Tateyama because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 8, Tateyama teaches converting the graphics data into a common format (see column 10, line 35).

As to claims 9, 11, 12, Tateyama teaches blanking out four-bit color data (0,1,0,0) (see column 9, line 1).

As to claim 10, Tateyama teaches the common format is selected from the group of YUV and RGB formats (see figures 13 and 14, column 3, lines 60-61).

As to claim 13, Tateyama teaches a graphic display system which includes a display engine "background Processing unit", a window controller "scroll box, superimpose box", a data packet (figure 28), a direct memory access "K-RAM" (figure 30, column 9, line 53 through column 10, line 14).

Tateyama fail to teach a read pointer for scrolling image. However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a

first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Since a writer pointer increments in accordance with a clock synchronized with the input image data Vs (figure 11, column 22, lines 20-22). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the read pointer taught by Sokawa et al for a read timing disclosed in the display scrolling image system of Tateyama because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 14, Tateyama teaches the display engine "background processing unit" (figure 30, column 4, lines 40-41). Sokawa et al teaches displaying the graphics data starting at the read pointer (P_R) with the offset start time when horizontal scrolling will be carried out (see figure 12A to 12B, column 22, lines 23-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the read pointer taught by Sokawa et al for a read timing disclosed in the display scrolling image system of Tateyama because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the

image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 15, Tateyama teaches a direct memory access "K-RAM" (column 4, lines 40-41).

As to claim 19, Tateyama teaches the first non-blanked out pixel is a first pixel is displayed (see figure 7, column 2, line 36-37).

As to claim 21, Tateyama teaches a graphic display system which includes a display engine "background Processing unit", a window controller "scroll box, superimpose box", a data packet (figure 28), a direct memory access "K-RAM" (figure 30, column 9, line 53 through column 10, line 14).

Tateyama fail to teach a read pointer for scrolling image. However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Since a writer pointer increments in accordance with a clock synchronized with the input image data Vs (figure 11, column 22, lines 20-22). Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the read pointer taught by Sokawa et al for a read timing disclosed in the display scrolling image system of Tateyama because this would minimize the total size circuit

configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 22, Tateyama teaches a direct memory access "K-RAM" (column 4, lines 40-41).

As to claim 23, Tateyama teaches the first non-blanked out pixel is a first pixel is displayed (see figure 7, column 2, line 36-37).

As to claim 24, Sokawa et al teaches the display engine "background Processing unit" for blanking out one or more pixels from a second input buffer portion by selectively placing the read pointer (Pr) (figure 12D, column 22, lines 51-58).

Response to Arguments

4. Applicant's arguments filed 8/6/2003 have been fully considered but they are not persuasive.

In response to applicant's argument that claims 1 and 7 recite "a data packet that includes a field for a blank start pixel value, which indicates a number of pixels to be blanked out; blanking out one or more pixels at a beginning of a portion of graphics data are blanked out in accordance with the blank start pixel value by placing a read pointer at a location after said one or more pixels," at page 9, 4th paragraph. This argument is not persuasive because Tateyama's invention teaches receiving a data packet (Y0 Y1 U0 V0) (figure 28) that includes a field for a blank start pixel value (Y0 U0 V0), which indicates a number of pixels to be blanked out; blanking out one or more pixels (Y0 U0 V0) at a beginning of a portion of graphics data in accordance with the blank start pixel

value; displaying the graphics data starting at a first non-blanked out pixel in the portion of the graphics data aligned with the start address (see figure 22, column 9, lines 1-20). Sokawa et al's invention teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

In response to applicant's argument that claims 13 and 21 recite "a window controller for transmitting a data packet to the display engine, the data packet including a field for a blank start pixel value, which indicates a number of pixel to be blanked out. The display engine is capable of selectively blanking out one or more pixels from a portion of the raw graphics data in accordance with the blank start pixel value by placing a read pointer at a first non-blanked out pixel after said one or more pixels and within said portion," at page 10, 1st paragraph. This argument is not persuasive because Tateyama teaches a graphic display system which includes a display engine "background Processing unit", a window controller "scroll box, superimpose box", a data packet (figure 28), a direct memory access "K-RAM" (figure 30, column 9, line 53 through column 10, line 14). Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines

27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

For these reasons, the rejections based on Tateyama and Sokawa et al have been maintained.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
October 3, 2003

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600